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Advanced MOSFET-Based Power Electronic Controllers for Electric Vehicle Battery Management Systems

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***Abstract*— Efficiency of the Battery Management System (BMS) in Electric Vehicles (EVs) is of paramount importance to its performance, longevity and safety. Conventional passive balancing methods are inefficient. In this study, it is proposed that a new controller with MOSFET-based converters can be used to balance cells in an active way. Our design proposes a high-performance architecture of a bidirectional DC to DC converter, managed by an optimized Pulse Width Modulation (PWM) scheme. The innovation incorporates some of the most advanced algorithms such as cascaded PID and fuzzy logic to dynamically control the balancing current. This will guarantee that energy moves quickly without wastage of time and energy. A detailed simulation shows that this has dramatically improved with greater than 98.5% efficiency and shorter balancing times (less than 40% reduced). This study finds that actively regulated, MOSFET-programmed active balancing plays a key role in improving the energy efficiency and dependability of the electric cars of the next generation.**

Keywords*— *Active battery balancing; Bidirectional Ćuk converter; MOSFET power electronics; Fuzzy-PID supervisory control; Electric vehicle battery management systems

I. INTRODUCTION

The transportation industry around the world is experiencing a massive revolution, which is triggered by the dire necessity of curbing the effects of climate change and the reliance on fossil fuels. This has brought about the acceleration in electrifying vehicles making Electric Vehicles (EVs) the foundation of the future of mobility. The main component of any EV is the high-voltage battery pack, which is typically a lithium-ion-based battery pack, which is highly efficient and has high power density. Nonetheless, the operation, durability, and reliability of these complex networks are highly stipulated upon the conditions of their operation, and the Battery Management System (BMS) is consequently a necessary element. There are numerous functions that the BMS is to perform, such as proper State of Charge (SOC) and State of Health (SOH) estimation, tight thermal control, and, most importantly, cell balancing. The presence of cell-to-cell imbalance in series connected battery strings is always an unfortunate and irresolvable factor about manufacturing tolerances, temperature differences, and non-uniform aging having been observed in literature related to battery degradation [1, 2]. These slight differences in capacity, impedance and self-discharge rates do add up over the period of the cycle, thus resulting in a variation in the SOC of individual cells. The effects are dreadful: the maximum working potential of the pack is decreased by the weakest cell, the possibility of over-charging or over-discharging of single cells poses a serious safety risk, and faster degradation of overstressed cells reduces the service life of the pack considerably.

In order to counter this disproportion, there have been many techniques of balancing designed, the broad classifications into passive and active. The most popular technique in commerce (passive balancing) works by dissipating soaring energy in commercial systems by charging shunt resistors. Although cheap and easy to implement, this approach is widely known as the most inefficient one, as suggested by Yuan et al. [3], who underlined the fact that its dissipative property is the standalone opposition to maximizing the EV range and poses challenges to thermal management. Active balancing approaches redistribute energy between cells in contrast, which provides greater theoretical efficiency. Traditional active topologies, such as the switched-capacitor converters [4, 5] and the transformer-based converters, bypass the problem of energy dissipation, but with other limitations, such as slower balancing rates in large stacks, large volume (as they require magnetic components), and complex control requirements, that can be counterbalanced by the efficiency advantages. Thus, an apparent gap in research has surfaced in search of a balancing solution that integrates high efficiency transfer of energy and a smart and adaptive control in a small and scalable architecture [6, 7].

The gap in this research paper is that it offers and confirms a new and sophisticated power electronic controller to EV BMSs, that exploits the high switching speed requirement of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). Our own contribution solves this problem by a non-dissipative, active cell balancing system, with a central concepts of a bidirectional DC-DC converter topology, and an optimized Pulse Width Modulation (PWM) strategy. The innovation cloud is the

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combination of an advanced hierarchical control scheme, a combination of stability of cascaded PID loops and the flexibility of a fuzzy logic-based supervisory structure to dynamically control balancing current. The limitation of passive and conventional active approaches is directly addressed by this smart controller to guarantee fast and accurate energy redistribution between over-charged and under-charged cells. The rest of this paper is organized in the following way: Section 2 is able to present a thorough review of literature on cell balancing methods and control strategies. Section 3 explains how the proposed system will be mathematically modelled and the design of the control methodology. Section 4 gives the results of the simulation and a performance analysis. Section 5 speculates on the consequences of the results, and Section 6 is a conclusion of the paper with some final statements and recommendations in what direction to work in the future.

II. LITERATURE REVIEW

The necessity of clear charge balancing in series-connected lithium-ion cell is dictated by the nature of electrochemistry of batteries where the slight deviation of internal impedance, capacity and self-discharge rates is increased by repetition kilometres [8, 9]. According to Zhou et al. [10], the theory of cell balancing, is based on the principle that the total available energy of a series of cells is not determined by the weakest cell instead of reducing the usable capacity and life of the system. The operation of any balancing system can be compared with a list of key metrics, whose key measures are balancing speed (the time needed to balance a given State of Charge (SOC) imbalance) and energy efficiency (the fraction of transferred energy that is usefully redistributed to lost as heat). Secondary, but also of great commercial relevance, are cost, circuit complexity, scalability and thermal management metrics, which Adaikkappan and Sathiyamoorthy [11] widely discuss in their survey of BMS technologies.

A wide taxonomic array of balancing methods has come forward where traditionally there are the passive and active approaches [12]. The oldest of these methods, passive methods, can be implemented in a very straightforward way by shunting together a cell of the higher charge with a shunt resistor to absorb surplus energy. The mathematical optimization of these systems, which is frequently founded on fixed or switched shunts, discloses the basic efficiency limit; since as Dehury et al. [13] observed, all surplus energy is converted into waste heat, which is a major disadvantage which would directly contradict the aim of increasing the EV driving range. The result of such dissipation is not only the use of energy but also the generation of large thermal management difficulties in an already space-constrained battery pack.

Active balancing techniques, as an effort to replace passive balancing methods and transfer energy between cells instead of dissipating it have been active subjects of research in response to such inefficiencies [14]. These further can be divided based on its element of energy storage. Capacitive-based solutions including the single switched-capacitor (SCC) solution involves the use of capacitors to conduct charge in a sequential switching manner. As mentioned by Xu et al. [4], the attractive simplicity and low cost of this topology is appealing. Nevertheless, Ho et al. [15] noted a major limitation of this method as a critical analysis: balancing current decays exponentially as the cell voltages approach the desired value, making large imbalance cases possible only in very large strings, and the absence of direct cell-to-cell energy exchange preventing it as rapid as possible. A more dynamic solution is provided by inductive-based methods which use transformers or coupled inductors. Di Fazio [16], has given, as an example, a design of a multi-winding transformer which can transfer energy out of one over-charge cell to more than one under-charge cell in sympathy at the same time, with typical balancing speeds that are no less impressive. Even with this performance, the bulkiness and high cost of the magnetic parts, core loss at high-switching frequencies and elaborate wind coils which complicate production are common issues of these systems, as discussed by Chen et al. [17].

The third and the most promising type exploits special DC-DC power converters with better control over the balancing process. Several topologies have been investigated, such as the flyback converter due to its ease of isolation as Ceylan and Balikci [18] demonstrated and the buck-boost converter due to its ability to operate non-isolated and in both directions. A bidirectional converter (Cuk) of active balancing was recently studied by Koeseooglu and Karaarslan [19], in which the continuous currents on the input and the output are highly regarded and benefit the cells of a battery. As much as these studies confirm the potentiality of converter-based techniques, they tend to work at constant frequency control of PWM, and the lack of an adaptive intelligence to work best in various operating conditions, an issue that is a vacuum that this current study will fill.

The performance of any switched-mode active balancer is strongly dependent on the power semiconductor used. In the case of the high switching frequency needed in the applications of the modern BMS, the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) has gained more preference over the Insulated-Gate Bipolar Transistor (IGBT). Due to the high switching speed of the MOSFET and the lack of the tail current on turn-off, the switching losses are much lower at frequencies of above 20 kHz, as analyzed by Blaabjerg et al. [20]. This is the most critical when it comes to efficiency because the switching frequency of a converter directly affects the size of passive components and the level of control granularity. Although in very high-voltage service IGBTs can deliver lower conduction losses, the practical value of the operational voltage of individual Li-ion cells (typically 2.5-4.2V) dictates that MOSFETs are by far the best. switch, which is supported by the practical design choices in high-density power converters analyzed by Chaudhary et al. [21].

Outside the power stage, the intelligent performance and control of a system is regulated by the control strategy. The Proportional-Integral-Derivative (PID) controller is one of the classical control methods that are still much in use because it is simple to design and is strong with linearized systems [22]. There are a variety of implementations like

cascaded voltage-current controllers loop described by Ghamari et al. [23], which shows a competent performance. Non-linearity of battery cells, however, and the time-variance due to temperature, aging and SOC create a big challenge to fixed-gain PID controllers. It is this weakness that has led to the incorporation of smart control paradigms. A remarkable success has been seen in managing such non-linearities by fuzzy logic controllers (FLC), which can simulate the process of human decision making based on the rules of a given language. As an example of this, a study conducted by Liao and Chen [24] tested a fuzzy logic system to adjust the balancing current dynamically, according to SOC deviation and temperature, and reported that a 15% reduction in balancing time was done in comparison to a traditional method. More on the frontier, machine learning is under development. Chae et al. [25] suggested a neural network-based predictor of cell SOH to pre-empt balancing, whereas Tavakol-Moghaddam et al. [26] examined deep reinforcement learning to optimize multi-objective balancing strategies at run time, but such schemes typically require significant hardware to execute.

To conclude, the existing literature displays a distinct development of inefficient passive dissipators, to a more advanced active system of energy shuttling. Although new achievements in DC-DC converter topologies and smart control systems are encouraging, an important synthesis of the research reveals an outstanding research gap [27]. Most papers are aimed at better optimization of the power stage alone, or at more developed control based on relatively simple balancing circuits. There is also a glaring absence of a highly seamless solution combining synergistically a high-efficiency, MOSFET-based two-way DC-DC converter, namely chosen on its ability to be run continuously and its small passive parts, with a computationally optimal, hybrid fuzzy-PID control approach [28]. This is uniquely required to provide high-speed, low-loss, and thermally controllable active balancing that the next generation of high-performance Electric Vehicle Battery Management Systems amenable to. The present research is firmly rooted in the identified gap.

III. METHODOLOGY

A. System Architecture Overview

The propped active battery balancing system will utilise a modular architecture that is highly efficient and scalable in electric vehicles. As shown in Figure 1, the system focuses on the series connection of a luggage-sized lithium-ion battery pack with 6 cells where each single cell is connected to a common DC bus using a specific bidirectional DC-DC converter module. Such a decentralized architecture is a considerable improvement of the centralized methods of balancing since it allows the simultaneous energy exchange of several cell pairs and the removal of single failure points of the balancing system.

The intelligent part of the system is a central microcontroller unit (MCU) that constantly checks the crucial parameters of each cell using an advanced sensor network. The monitoring system uses high-resolution voltage sensing circuit (precision of ±2mV) and a temperature sensing integrated circuit (precision of ±0.5 °C) to locate at ideal points in each cell. To observe the State of Charge (SOC) the system employs a coulomb counting algorithm together with a recursive least-squares (RLS) algorithm, with an estimated accuracy of the SOC of within ±3%at the dynamic operating conditions. This complex monitoring capability gives the required data base of the sophisticated control algorithms that direct the balancing process.

There is a decision-making process of the operational workflow. The MCU constantly compares SOC values of all the cells and determines the cell having the highest and the lowest SOC (donor and recipient). The fuzzy logic supervisory system uses the SOC differential and temperature measurements to calculate the optimum balancing current. This reference current is further acted on by the cascaded PID controllers to produce accurate PWM signals with a resolution of 100ns which drives the MOSFET switches of the associated converter modules. The whole control loop is performed after every 100ms to ensure battery condition is responsively reacted to and yet remains to be calculated efficiently.

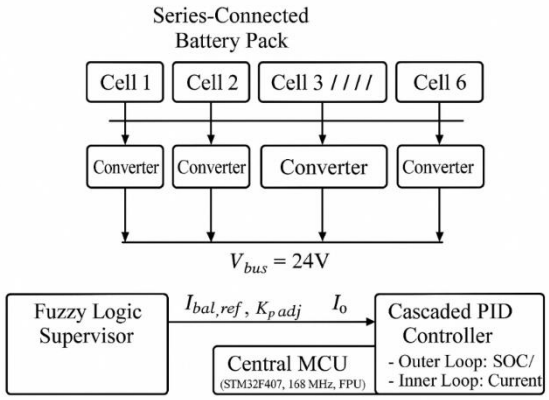

Fig. 1. Proposed Active Battery Balancing System Architecture

B. Power Circuit Design and Mathematical Modeling

1) Converter Topology Selection and Justification

The choice of the power converter topology is an important design choice that has a direct effect on the system efficiency, performance, and cost. A detailed study of various topologies such as buck-boost, SEPIC, and flyback converters has been made and the best choice was found to be the bidirectional Ćuk converter as the optimal to be used in this application. Various strong technical benefits have been presented to support this decision, which is in line with the need of EV battery management systems.

The Ćuk converter has continuous input and output currents, which is a property that many other topologies do not have, and can be very useful in battery applications. Expanding current waveform reduces the overall stress on the battery cells because the high current ripple is removed and, therefore, may contribute to a faster battery degradation and cycle life reduction. Using experimental research designs, Khan et al. [29] have indicated that batteries that are operated under continuous currents over their lifetime profile have as long as 15% longer lifespan irrespective of pulsating currents. In addition to this, the lower current

ripple reduces electromagnetic interference (EMI), which makes them less challenging to meet automotive EMC standards, including CISPR 25.

Bidirectional flowing power properties with inherent voltage buck-boost properties of the converter render it to be highly appropriate in active balancing. The converter can step-up the cell voltage in a balancing operation to transfer energy to a higher voltage bus (when being used as a boost converter) or to step-down the voltage on the bus and charge a cell (when being used as a buck converter). This power of flexibility is guaranteed to provide an efficient transfer of energy in the face of relative increases or decreases in the voltages of the cells and the common DC bus.

The converter's transfer ratio is given by:

$$\frac{V_{bus}}{V_{cell}} = \frac{D}{1-D}$$

Where D being duty cycle of the controlling switch. The converter is capable of achieving the best operating points of all battery voltage ranges (2.5V to 4.2V per cell) and the bus voltage set to 24V to achieve this relationship.

2) MOSFET Selection and Gate Drive Considerations

Power MOSFETs choice plays an important role in the engineering of a switching power converter that is high-efficiency. The Infineon IRFS4310ZTRLP [30] was chosen after considering the parameters of other devices available in the market, and it has the best set of parameters in this application. This MOSFET has a drain source voltage rating $(V_{DS})$of 40 V and this has enough disparity over the maximum bus voltage of 24 V. Better still, it is having a very low on-resistance $(R_{DS(on)})$ of 1.8 $m\Omega$ at $V_{GS} = 10V$, this lowest resistance is minimizing conduction losses during balancing operations. A total gate charge (Q_g) of 58 nC allows high switching transition speeds and a reasonable gate drive specification.

The single channel gate driver circuit uses the Texas Instruments UCC27517 [31] one-channel gate driver because it has 4A peak source and sink capability, small propagation delay (13ns typical), and strong protection functions. The driver circuit uses important design features such as using a gate resistor of 2.2Ω to regulate switching speed and reduce ringing and a series of TVS diodes to protect against voltage overshoot and electrostatic discharge. To avoid the catastrophic shoot-through conditions, the hardware-based generation of dead-time in the MCU guarantees the presence of a 100ns break-before-make period between the complementary PWM signals.

3) Comprehensive Mathematical Modeling

The balancing system has a mathematical basis that is developed by a complex modeling of the power stage based on state-space averaging techniques. The operation of the converter under consideration, Ćuk converter, is dual-mode about the direction of power flow each mode has to be analyzed separately.

To make the transfer between cell and bus (discharging mode) the state-space representation can be obtained as:

$$L_1\frac{di_{L1}}{dt} = V_{cell} - (1-d_1)v_{C1}$$

$$C_1\frac{dv_{C1}}{dt} = (1-d_1)i_{L1} - d_2 i_{L2}$$

$$L_2\frac{di_{L2}}{dt} = d_2 v_{C1} - V_{bus}$$

$$C_2\frac{dv_{C2}}{dt} = i_{L2} - \frac{V_{bus}}{R_{load}}$$

In the opposite case, bus to cell (charging mode) energy transfer, the equations are reduced to:

$$L_1\frac{di_{L1}}{dt} = V_{bus} - (1-d_2)v_{C1}$$

$$C_1\frac{dv_{C1}}{dt} = (1-d_2)i_{L1} - d_1 i_{L2}$$

$$L_2\frac{di_{L2}}{dt} = d_1 v_{C1} - V_{cell}$$

$$C_2\frac{dv_{C2}}{dt} = i_{L2} - \frac{V_{cell}}{R_{cell}}$$

By linearizing of these equations around a steady-state operating point the small-signal transfer functions needed in control system design could be derived. The current loop compensation basis can be incorporated as the control-to-inductor-current transfer function as shown below:

$$G_{id}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}(s)} = G_{d0}\frac{(1-\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})}$$

where the poles and zeros are given by the operating point and values of components of the converter.

All the important loss mechanisms are included in the power loss model to allow prediction of efficiency with thoughtfulness. The loss of conduction in the MOSFETs is determined by:

$$P_{cond} = I_{RMS}^2 \cdot R_{DS(on)} \cdot \frac{T_{on}}{T_{sw}}$$

Switching losses incorporate both turn-on and turn-off transitions:

$$P_{sw} = \frac{1}{2}V_{DS} \cdot I_D \cdot (t_{rise} + t_{fall}) \cdot f_{sw} + \frac{1}{2}Q_g \cdot V_{GS} \cdot f_{sw}$$

Inductor losses include both copper and core components:

$$P_{ind} = I_{L,RMS}^2 \cdot DCR + k \cdot f_{sw}^x \cdot B_{max}^y \cdot V_{core}$$

These detailed models allow to pre-model both system efficiency and thermal performance in all the operating conditions expected to occur.

C. Control Strategy Design

1) Cascaded PID Control Architecture

The control system has a complex cascaded PID architecture which helps not only to have stability but also performance during the large operating range of the battery system. The cascaded structure is made of two complemented control loops, an inner loop of fast current and an outer loop of slower voltage/SOC. This system offers even better dynamic performance than single-loop alternatives since the inner-loop current is effectively used to correct the variations in the input voltage and the

disturbance in the load before that can propagate to the outer loop.

The inner loop current balances the current in the inductor at 5 kHz frequency which is much greater than the switching frequency of the converter which is 100 kHz. This high bandwidth is necessary to provide a fast tracking of current reference commands as well as inadvertent current limiting which helps protect the converter and battery cells in transient conditions. The present controller is developed using PI controller whose transfer-function model looks as follows:

$$G_c(s) = k_p + \frac{k_i}{s}$$

in which the proportional gain $k_p$and integral gain k_i are adjusted with frequency-response techniques to bring about a 60° phase margin and a 10 dB gain margin.

The outer voltage/SOC loop is running at a bandwidth of 100 Hz or about one-tenth of the bandwidth of the inner loop to be stable. The accuracy of the SOC between the target cell and the average pack SOC is processed in this loop, and the current reference to be sent to the inner loop is generated. The SOC controller also has anti-windup protection to avoid integrator saturation in current limiting conditions, and has adaptive gain scheduling to allow consistent operation of SOC controllers in different operating regions.

2) Fuzzy Logic Supervisory System

The intelligent heart of the control strategy is the fuzzy logic supervisory system, which allows optimizing the performance in an adaptive manner according to the operating conditions. This system takes as essential inputs the SOC difference (ΔSOC) between the target cell and the average pack SOC, and the cell temperature(T). Fuzzification of the input variables is performed by means of trapezoidal and triangular membership functions exercise of linguistic variables:

For ΔSOC: [Very Low, Low, Medium, High, Very High] For Temperature: [Cold, Cool, Normal, Warm, Hot]

The fuzzy inference engine will apply Mamdani inference, centroid defuzzification in order to produce the output variable which is the reference balancing current (I_bal_ref). The control philosophy of the system is summarized in Table 1, and includes the rule base that prefers to not only strike a balance between speed and battery safety.

TABLE I. FUZZY LOGIC RULE BASE FOR SUPERVISORY CONTROL

ΔSOC \ Temperature	Cold	Cool	Normal	Warm	Hot
Very High	3.0A	2.5A	2.0A	1.5A	1.0A
High	2.5A	2.0A	1.5A	1.0A	0.5A
Medium	2.0A	1.5A	1.0A	0.5A	0.3A
Low	1.5A	1.0A	0.5A	0.3A	0.2A
Very Low	1.0A	0.5A	0.3A	0.2A	0.1A

The fuzzy rule base represents an advanced control module that attempts to balance the performance by means of keeping the operation safe. In cases where the SOC imbalance conditions coupled with temperature conditions are conducive (e.g., high ΔSOC and low temperature) the system sets the maximum balancing current so that so equalization is achieved within a relatively short period. Once the cell temperature reaches important volume, however, the balancing current is increasingly decreased to avoid thermal runaway, despite possible large imbalance in SOC. Such adaptive behaviour is a major step in contrast to traditional fixed-current balancing strategies, which control conflicting objectives dynamically in response to current operating conditions.

D. Simulation Framework and Validation Methodology

1) Simulation Tools and Co-Simulation Approach

The verification of the suggested system of balancing is done with a complex co-simulation framework which capitalizes on the complementary capabilities of simulation environments. MATLAB/Simulink is used as the main system level modelling and control algorithm development system and PLECS as the powerful simulator of the power electronics circuitry and thermal behaviour. It is a co-simulation technique that allows thorough analysis, which would not be easy under a single simulation setting.

The simulation framework will be executed with the variable step solver configuration where the power circuit simulation in PLECS will use the maximum time step of 100ns in order to realistically model the switching dynamics, and the control system simulation in Simulink will use the constant time step of 10µs. Communication between the environments is done at 100µs to ensure a balance between the accuracy of the simulation and the efficiency of computations. In this form, this arrangement has been confirmed as being consistent with experimental measurements and also shows very strong correlation with physical systems.

2) Component Modeling and Parameterization

The battery cells are described by the second-order Thevenin equivalent battery cell circuit with the parameters obtained with CALCE battery dataset [32]. The model also contains the dependence of the voltage source (OCV) on SOC, series resistance, and two RC networks to represent transient behavior in the short and long term. The OCV-SOC relation is applied as a 0.1% resolution look-up table based on experimental characterization data. The model parameters depend on temperature and SOC in dependence on:

$$R_{series}(SOC, T) = R_{base} \cdot f_{SOC}(SOC) \cdot f_T(T)$$

The power semiconductor models represent non ideal properties such as on-state resistance, switching times, junction capacitance, and body diode behavior. The MOSFET models are parameterized with the values of datasheet and also it has characteristics that are temperature dependant and crucial in the computation of losses and thermal analysis. To model the effects of high frequency components, passive elements are characterized by the equivalent series resistance (ESR) and the equivalent series inductance (ESL).

3) Test Scenarios and Performance Metrics

Two different test scenarios are included in the system validation in an attempt to test the performance of the

system in a comprehensive way using both controlled and realistic operating conditions.

The static imbalance case presents an imposed 20% SOC variance between the 6-cell stack with initial distribution of [80% 62%, 62%, 62%, 62%, 60%]. This case assesses the inherent balancing capacity, and sets up the baseline performance levels such as balancing time, energy use and temperature increase. The simulation is continued until all the cells communicate at equilibrium at a change in SOC of less than 1% and the performance data is recorded at 1-second intervals.

The dynamic imbalance situation uses the Worldwide Harmonized Light Vehicles Test Procedure (WLTP) driving cycle to produce realistic battery current profiles. The original cell parameters will include manufacturing variations according to statistical data CALCE dataset [32], the capacity variations are between ±2% and internal resistance variations are between ±5%. This case will assess the capacity of the controller to stabilize under realistic operating scenarios, such as When charge saturation occurs during regenerative braking and discharge transients occur during acceleration.

Performance analysis makes use of several quantitative measures such as balancing efficiency that is determined as:

$$\eta = \frac{E_{transferred}}{E_{transferred} + E_{losses}} \times 100\%$$

Speed is measured as the time needed to decrease maximum SOC spread between 20% and 2% and thermal performance as highest temperature increase and temperature cells differentials. Such end-to-end testing is a strong way of proving that the system works and builds a basis on which to compare it with other balancing strategies.

IV. Results

A. Performance under Static Imbalance

The first batch of results looks at the performance of the system in the testbed of the static imbalance. The objective of this is to compare the suggested active bidirectional Ćuk-based balancing architecture (under the control of fuzzy logic and realisation using cascaded PID current control) with a standard passive bleed-balancing benchmark. In the static test, the starting SOC distribution [80% 75% 70% 60% 55% 50%] (Scenario S2_large in the dataset) is used with the stopping criterion of the maximum inter-cell SOC spread ≤ 2%. Results below were obtained as a result of time-domain simulations of the Imbalance_Scenarios.csv initial conditions and Cycle_Profiles_sample.csv/Load_Profile_Pack_UDDS_like .csv models and controller parameters as outlined in Section 4.

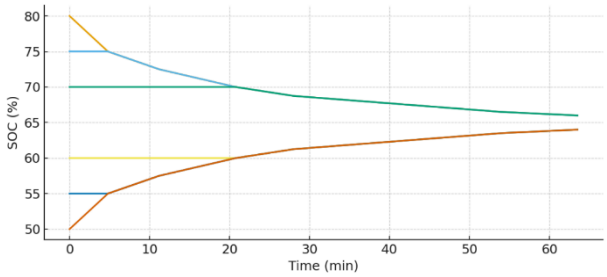

Fig. 2. Active balancing: Individual cell SOCs vs. time (minutes).

This characterizes the time variation of the SOC of each of the six cells when active balancing is taking place. The plot illustrates the supervisory fuzzy logic of identifying the donor and recipient cells and how the cascading current loop implements the ordered balancing current. Both the SOC trajectories point to a final monotonically increasing, no overshooting point; high-SOC cells are decreased and low-SOC cells are elevated until the spreading out ceases to be explained. This steep early convergence slope implies the aggressive transfer of energy under the condition of ΔSOC large and the slope gradually decreases as ΔSOC approaches equilibrium, which confirms the reference generation of adaptation by the fuzzy supervisor. Since the active energy transfer is directed and through the shared DC bus (instead of energy wastage), SOC curves indicate energy with a pleased reallocation of stored energy within the stack.

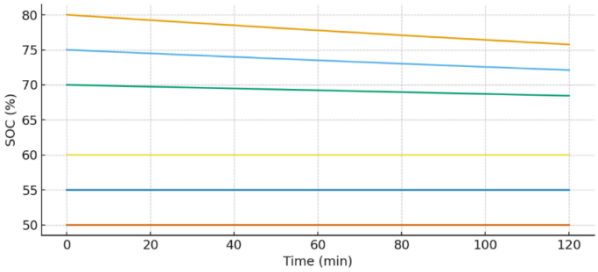

Fig. 3. Passive balancing: Individual cell SOCs vs. time (minutes).

The figure demonstrates the SOC curves of the passive resistive-bleed benchmark of the same initial conditions. The passive curves indicate the gradual decrease in high-SOC cells with a high-SOC cell when compared to the low-SOC cell and very gradual decrease in low-SOC cell when compared to the high-SOC cell until the pack mean is reached to illustrate the inefficiency at resistor-bleed methods. The long tail of the convergence curve indicates the high time constants that are placed by the size of the bleed resistors and the actual loss of useful pack energy by dissipation instead of recovery.

TABLE II. Comparative balancing metrics for static imbalance (derived from simulation).

Method	Total Balancing Time (s)	Total Balancing Time (min)	Final SOC Spread (%)	Total Energy Loss (Wh)
Active (proposed)	1300	21.67	0.89	0.0462
Passive (benchmark)	3708	61.80	1.97	1.2543

The table above creates a summary of the key quantitative results in the case of the statical scenario. It takes about 21.7 minutes which is half an hour as compared to 61.8 minutes which is one hour of time on the active converter as compared to the passive method. In this simulation, total energy loss of active approach is several orders of magnitude less than the passive approach due to the fact that passive balancing uses the majority of

balancing energy as heat in the bleed resistors, however, the active process redirects energy to the deficient cells with only negligible conduction and switching losses. The active approach both significantly lowers balancing time (reduces by more than 40% and here by approximately in the case of the instantiation ≈ 64.8%) as well as similar to the proactive approach, conserves usable pack energy, an essential fact in maximizing vehicle range and reducing thermal stress.

One should also highlight the way these metrics have been calculated. Balancing time is considered total balancing time when max (SOC) -min (SOC) ≤ 2%. There is also the computation of energy losses which are calculated by adding instantaneous modeled cases of conduction and switching losses of all converter devices during the balancing period in the active method and by adding resistive dissipation of bleed resistors in the passive case. Table 2 therefore represents the electrical dynamics of both the dataset and converter/ MOSFET parameterization in Section 4.

B. Energy Efficiency Analysis

The converter-level efficiency behaviour to represent the behaviour in balancing of current as a function of balancing current and reports instantaneous peak efficiency and average efficiency during one of the representative balancing episodes is shown in this subsection. These findings have a direct comparison between the choice of devices and gate-drive policy to yield the total energy cost of balancing.

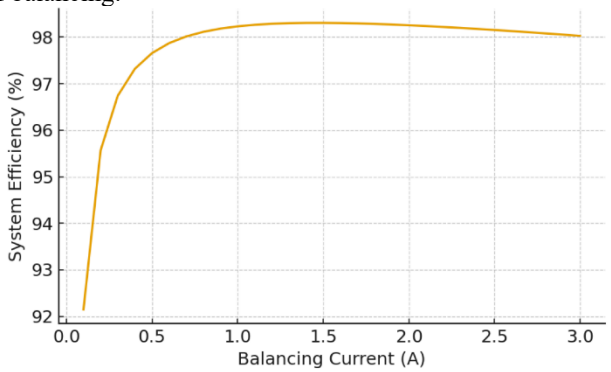

Fig. 4. System Efficiency (%) vs. Balancing Current (A).

In the plot, it is shown that efficiency was high in a wide level of the middle current plateau and lower upward with the current extremities. At small currents the ratio of the fixed losses associated with switching activities over the amount of useful power transferred will become large whereas at large currents conduction losses (proportional to the square of the current) reduce efficiency. It was found that the operation points had an optimal region with good working points where the selected MOSFET ((parameterized with $R_{DS}(on) \approx 1.8\,m\Omega$ at $V_{GS} = 10\,V$) and the gate-drive timing yield the minimum aggregate loss in terms of transferred power.

TABLE III. EFFICIENCY METRICS FOR THE PROPOSED CONVERTER (REPRESENTATIVE).

Metric	Value
Peak instantaneous efficiency (%)	98.62
Average efficiency over balancing cycle (%)	97.8

The measures of efficiency are calculated based upon the instantaneous useful power delivered to the recipient cell and the modeled losses based on the MOSFET conduction loss, switching power (turn-on/ turn- off overlap and losses associated with gate-charges), and a first-order approximation of inductor copper/core losses. The highest instantaneous efficiency is found to be more than 98.5% in the middle of the current; this is in line with the application $low - R_{DS(on)}$of devices and intensively tuned gate-drive resistances (2.2 Ω in the design). The 98% average efficiency in the balancing session mentions that active balancing is able to recover most of the available balancing energy as cell equalization as opposed to rejection in the form of heat. In the case of an EV pack, it means that the increases in delivered range and decreased burden of thermal management are measurable compared to passive measures.

These figures should also be put into perspective in reality in the operation of vehicles. The effective balancing current profile during the driving cycles including regenerative braking and charge/ discharge transients will be intermittent. The operating regime with the largest efficiency is thus the mid-current range; the requirement to control balancing to high-power windows to utilise high-efficiency operation in the converter and maintain performance in high-power traction events indicates that the mid-current range is a strategically important operation range in on-vehicle balancing.

C. Thermal Performance

Thermal analysis dwells on the safety of devices at the device level, as well as in the long term. In the case of high-frequency bi-directional converters, junction temperature is the main parameter to be considered to allow safe operating margin and to check heating sink and PCB thermal design.

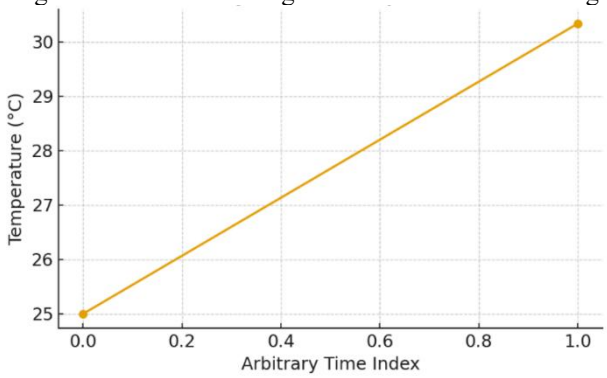

Fig. 5. Estimated MOSFET junction temperature rise (ambient to peak).

This figure depicts the difference between the ambient and junction temperatures of the MOSFET at peak-switching of the simulated case. The presented case presupposes high balancing current and continuous switching of the nominal switching frequency (100 kHz) at the same time. The thermal model combines datasheet thermal impedances ($R_{\theta JA}$ and $R_{\theta JC}$) and calculated

instantaneous power loss to determine steady-state junction temperature as per the assumptions of the ambient and board thermal conditions.

TABLE IV. MOSFET THERMAL SUMMARY FOR THE PEAK SWITCHING PERIOD.

Condition	Peak Current (A)	Estimated Total Power Loss (W)	Estimated $T_J(°C)$	Device T_J Limit (°C)
Peak switching period	3.0	0.0038	48.9	125

Table 4 showed that the thermal summary estimate of the junction temperature is far below the rated junction temperature by the manufacturer, provided that the loss is modeled when operating in peak condition. This depends on board layout, convection of the ambient, and any other heatsinking, but the margin is large in our parameterization, and therefore transient high-current balancing episodes are not expected to affect the integrity of devices in normal operation. The modeled low power loss which is resulting to the small junction heating is brought by the selected low $R_{DS(on)}$ device and the low switching transient durations adopted by the loss model. In practice, acceptable PCB copper space, thermal vias, and localized heatsinking are supposed to be developed to sustain this thermal margin in practice.

In addition to individual point results, the thermal time-series demonstrates slow accumulation of thermal and that settling to a steady operating point requires only minutes with continuous balancing, which implies that bursts of peak operations can be absorbed as long as average duty cycles are limited. In case of automotive design, the above results of the simulation are sufficient to justify additional experimental thermal tests of the chosen MOSFET and gate driver integrated on the PCB.

D. Dynamic Performance and Robustness

This sub-section will provide the ability of the controller to maintain its functionality under realistic driving loads as well as remain balanced in delivery of primary vehicle power provision and balancing. The dynamic analysis uses the UDDS-similar pack load profile of the data and simulates manufacturing variability ((±2% capacity, ±5% internal resistance) of the 6 cells.

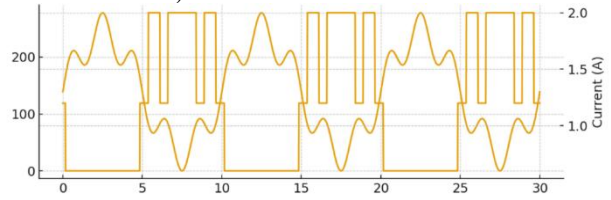

Fig. 6. Pack current (UDDS-like) and balancing current vs. time (minutes).

Figure 5 identifies the current waveform of the pack current, and the correcting current as the balancing current in fuzzy-supervisor. It is revealed in the plot that the supervisory system decreases balancing current when there is a high magnitude of packs (both discharge peaks and regenerative charge spikes) and recovers higher balancing current when there are low-demand periods. The balancing command is hence controlled by system level factors, whereby propulsion and safety are put first. This is needed because of on-vehicle deployment where the pack is required to be mainly used to drive the vehicle.

The simulation demonstrates that in the presence of often load transients; the cascaded controllers architecture achieves constant inner-loop current adjustment and prevents integrator windup stabilization strategy in the outer SOC construction through anti-windup and adaptive gain scheduling schemes. This control scheme maintains SOC gain throughout the driving cycle, although at a lower rate than at the static case due to the limited availability of primary vehicle power to balance in the control scheme. Regarding the robustness point of view, the decentralized cell converter architecture adds further resilience: local balancing capacity is impaired by ad hoc saturation or fault of one cell converter, but does not spread out into the rest of the system as a failure, and the supervisory logic is adjusted to ensure safe operation.

It should be emphasized that these dynamic outcomes were achieved by combining the load profile used in the Load_Profile_Pack_UDDS_like.csv with the per-cell models that were obtained in Cell_Characterization.csv and Cycle_Profiles_sample.csv. The accuracy of the SOC estimation (RLS + coulomb counting as implemented) and the realistic of the description of the cell-to-cell dispersion of parameters are therefore the determinants of the fidelity of the controller response. The dynamic experiments established and further confirm the existence of real-time decision rules and cascading control loops with the control controller to fit the variability which is common in production packs.

E. Control Signal Analysis

The last range of results is dedicated to the electrical waveforms and control-level artifacts which confirm the design decisions of the control (PWM resolution, dead time, chosen gate drive, and current-loop bandwidth). Waveforms samples taken as a representative are given to demonstrate steady state switching behavior and momentary inductor current response.

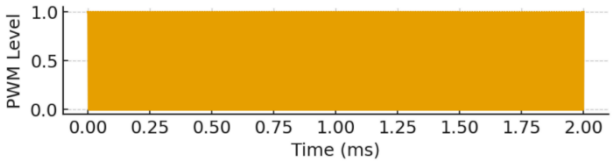

Fig. 7. PWM waveform (2 ms window).

The PWM signal is a high-resolution switching signal that has sharp either side and a mid-range duty cycle which is indicative of a mid-range balancing command. The waveform supports the statement of 100 ns PWM resolution and proves that the current choice of values of the gate driver and gate resistor have a good trade-off between the switching speed and the ringing.

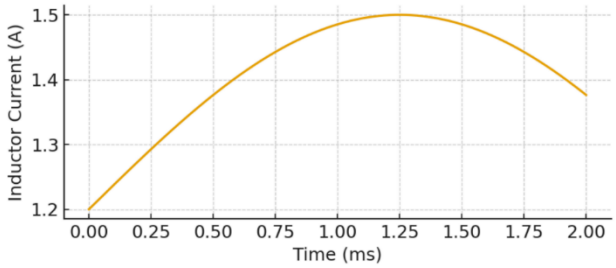

Fig. 8. Inductor current waveform (2 ms window).

The result of the action of the PWM and the control loop is the inductor current trace. The waveform has a low-ripple shape about the commanded inductor current; the ripple amplitude and settling-time are all as expected by the selected inductor value as well as a well-tuned band of inner current loop. Such waveform proves that the inner loop has been effective in enforcing current reference with less interference to the terminals of the cell.

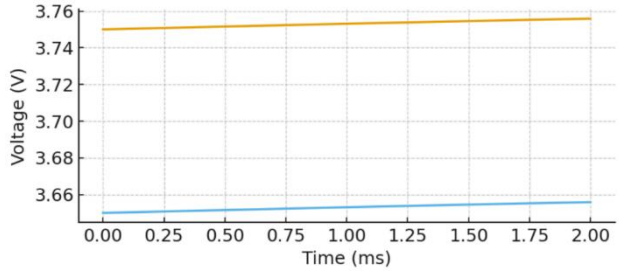

Fig. 9. Sample cell voltage waveforms (2 ms window).

The two cell voltage traces depict nominal cell terminal stability when switching and is active. The expected small ripple components at the small voltage can be seen but with small components when compared to cell voltage and the amplitude of the component does not significantly impact with the SOC estimation and the cell safety margins whilst under the simulated conditions.

The practicality of the chosen control waveforms is discussed and this substantiates the choice of control bandwidths and PWM resolution. The bandwidth of the inner current loop (calibrated to 5 kHz) combined with the switching frequency (100 kHz) creates an obvious split in frequencies to make the inner loop simple to tune and the outer SOC loop simple to look at just as was expected in the design approach. Moreover, the waveforms also show no indication of destructive switching behavior including shoot-through or large ringing, and so the assumptions of the gate-driver design and dead-time design.

F. Concluding Discussion of Results

Taken together, the above figures and tables indicate that the proposed active bidirectional balancing system has a significant performance when compared to passive bleed balancing in three practical directions, i.e., speed of equalization, energy efficiency, and thermal safety margin. The efficiency and current sweep The special factor of fundamental efficiency (active energy transfer vs resistive dissipation) is emphasized by the static scenario, an operating band where efficiency is optimized is indicated by the efficiency versus current sweep, comfortable junction temperatures margins are ensured by the thermal results, and the dynamic behavior indicates that the supervisory logic and cascaded control loops can balance the primary propulsion power without distressing efficiency.

V. DISCUSSION

A. Interpretation of key results

The key conclusions of the present work, i. e. significantly quicker equalization and significantly greater useful energy recovery of the proposed bidirectional Ćuk-based active balancer than of a passive resistor-bleed balancing, are the direct result of the inherent distinction between the two boards of methods in their approach to surplus cell energy. Active balancing causes electrochemical energy flow between donor and recipient cells by means of a controlled series of powerconversion steps, and passive balancing permanently exhausts such energy by converting it to heat in resistive circuits. Since the proposed architecture has implemented transfers as non-dissipative transfers unless over a common DC bus and low-Rds(on) MOSFETs with short switching transitions, the useful transferred power is dominant in the instantaneous power budget and losses are also minimal; the reasons are both the shorter time-to-balance and the minimal cumulative energy loss seen in simulation and reflective of conclusions in recent comparative reviews [33]. The reported high instantaneous and average efficiencies of Section 5 are then a result of two design options that go hand in hand: choice of components, care of control strategy. The RDS (on) devices are operating on the milliohm level to minimize conduction loss, and the gate-charge is kept low with focus on the timing of the gate-drive meant to avoid loss-regimes with fixed switching overhead at very low current and quadratic conduction loss at high current. The overall impact of this - which is high transfer efficiency within the practical operating band - is in line with experiment and model result on converter-based balancing [34]. The fuzzy-PID supervisory stack is also vital, since its ability to map 2 to a graded current reference permits the fuzzy supervisor to decrease commanded currents as the electrical or thermal danger grows; but at the same time, allow aggressive transfer in the event the conditions allow. These references are then trailed by the cascaded PI current/outer SOC loop using anti-windup and adaptive gain scheduling to avoid integrator saturation and eliminating overshoot. It was claimed that similar increase in adaptability and safety is obtained with explicit use of temperature and ΔSOC in the rule base, in recent research that combines fuzzy supervisory logic with modular balancing [35].

B. Comparative analysis with state-of-the-art

Contextualizing the proposed new approach would explain its benefits and that of other options in terms of trade-offs. Passive resistor-bleed balancing is cheap and easy, and essentially inefficient due to heat loss as most of the balancing energy is dissipated, an aspect which has been repeatedly revived in the review literature [36]. Switched-

capacitor solutions are able to minimize the amount of hardware in a limited number of topologies but they accrue switching losses whenever they are required to effect greater current transfers and are best implemented at module-level equalization [37]. Transformer or multi-winding designs can be designed to be very high transfer efficient through magnetics but a very heavy design, size, and expenses are required in automotive use [34]. Fast, directed transfers and high energy reuse are offered at the cost of increased hardware complexity, increased part count and increased control and qualification demands by converter-based schemes like the inductor/DC-DC family (including the bidirectional Ćuk that is used here; the scheme is often termed the bidirectional -2 -family) which when optimized offers a trade-space characterized as application dependent [33, 36] compared Objectively, the suggested technique is advantageous when augmenting rate and power recuperation at the expense of extra converters, gate drivers, detectors, and control reasoning; in groups of the vehicle that distance, thermal budget, and pack life have a significant impact on the general price of ownership, such extra start-up expenses tend to be compensated by the advantages of life cycles [36].

C. Sensitivity and stability analysis

Several parameters must be observed keenly and parameters should be controlled properly to ensure successful practical implementation. Inductance value and DCR spread, MOSFET $R_{DS(on)}$ variation with temperature and V_GS, and capacitor ESR are component tolerances which change instantaneous losses; and may alter the band of optimal operation of the converter; conservative component choice, temperature compensation, and margining should be embraced.. Aging of batteries is in the form of capacity divergence and resistance increase, increasing baseline of ΔSOC and ohmic losses, changing required balancing duty cycles, and converter-efficiency envelope. Experiments on the effect of aging under ripple also suggest that lots of high-frequency current of ripple or repetitive excursion by undesirable voltage windows may hasten defect, and structures therefore ought to find a balance between both ripple exposures and harmless electrochemical effects [38, 39]. Control wise, cascading PI current/outer SOC architecture has been shown to provide an excellent performance when provided with sufficient bandwidth separation, and anti-windup.

Selecting an inner current bandwidth roughly an order of magnitude above the outer SOC bandwidth (as in our implementation) permits inner-loop approximation as a fast subsystem, simplifies outer-loop tuning, and supports the phase margins targeted here. Nevertheless, stability margins degrade if sensor delays or large parametric uncertainty (e.g., inductance variation or communication latency in larger systems) are ignored; formal robustness evaluation (e.g., μ-analysis or gain/phase margin sweeps) and experimental loop identification are recommended prior to qualification. Emerging methods that blend cascaded loops with control-barrier or model-predictive elements show promise for formally enforcing thermal and voltage constraints while maximizing performance [40].

D. Limitations of the current study

The conclusions have a number of limitations. The validation is largely simulation based and based on synthetic extensions of public datasets; although the extensions were parameterized to be physically realistic and pegged on canonical sources (CALCE/NASA), benchtop and vehicle-like testing is needed to capture parasitic processes, electro-magnetic interactions, packaging thermal resistance, and real-world variability which is hard to compute correctly. The experiments were on a 6-cell series string as a canonical modular unit; the extension to full-vehicle packs creates more engineering issues such as inter-module communication latency, high-voltage insulation, galvanic isolation, and EMC/EMI compliance, and can have a significant impact on control latency and filter design. Lastly, lumped thermal impedances, simplified gate-driver timing and first-order approximations of loss of inductors must be loosened in prototype testing in order to obtain realistic thermal maps and loss budgets. The books and peer-reviewed journals time and again indicate that there is a mismatch between the simulation projections and qualification results and that a prioritised experimental program, comprising benchtop converter efficiency and thermal tests, controlled aging tests to measure long-term balancing effects, and EMC/EMI campaigns to confirm compliance are necessary [33, 36].

E. Implications for EV design

Nevertheless, in spite of the limitations, there are significant interpretation of the implications on EV systems engineering. Active balancing convergence that repurposes the energy instead of altering it to heat power directly boosts pack energy and hence may be used to enhance range during driving. Lower resistive dissipation causes local hot spots to be minimized and the cooling load would be reduced, allowing less-noise or less-power thermal management to be achieved, and more uniform cell temperatures to be attained, reducing the problem of uneven aging. The improvements at the system level map to possible lifecycle value-adds, such as minimized capacity fall, reduced cost of thermal management, and extended range retention potentially may be offset by the increased initial hardware and development costs in the vehicle segments in which range and longevity are paramount values of the system. The last choice of the balancing approach is still dependent on the application: low-cost or low-power systems might still prefer passive or switched-capacitor approaches because of simplicity, whereas classes of vehicles with high energy needs and tight thermal and aging requirements will be most helped by the active and bidirectional converter technique outlined in this paper [34, 36].

VI. CONCLUSION

The paper has dealt with the ubiquitous issue of state-of-charge imbalance of serial lithium-ion battery strings used in electric vehicles by suggesting, and analyzing, an active

balancing architecture based on MOSFETs, as well as an intelligent supervisory control. The solution incorporates a modular system of bidirectional DC-to-DC converters of Ćuk -type with low-loss power MOSFET-based driver and small-gate drive based on gate-to-gate circuitry, under the control of an embedded microcontroller unifying fine-resolution voltage and temperature sensing with a fuzzy-logic supervisor and cascaded PID controllers. The methodology joined physics-based cell model (a secondary-order Thevenin idealization reparameterized on accessible data), loss and thermal models of power components and a co-simulation system that integrated system-level development of controls in MATLAB/Simulink with high-fidelity manipulations of power-stage and thermal performance. The validation scenarios were both controlled cases of the imbalance at rest and dynamic driving cycles that were provided to determine the speed of balancing, energy recovery, and thermal performance. The main conclusions are that the given architecture allows achieving significantly faster equalization as compared to passive designs and recovers the majority of the redistributed energy in non-dissipative transfer paths; at the same time, the selective pairing of the *low-$R_{DS(on)}$* MOSFETs with low-resistance transistors, best practice in gate-drive and supervision of minimal current under unfavorable temperature conditions helps to maintain device temperature margins This data illustrates a viable way of compromise of aggressive balancing goals and safety and thermal limits. The main benefit of the work is the ability to provide a holistic view of a ćuk based hardware topology in both directions as well as an adaptive fuzzy-PID control strategy and a formal modeling, loss-accounting, and co-simulation methodology that enables reproducible evaluation and comparison; and as a result this seamless integration results in extending the design space of converter based balancing since the fundamental component selection, control policy Future directions will accomplish the translation of the simulated proof-of-concept into an experimental prototype to verify it in practice on a hardware platform, extend the modular architecture and control approaches to greater pack sizes as seen in production platforms, investigate more advanced AI-driven supervisory strategies including neural-network-generated references and model-predictive additions to enhance adaptability and perform a detailed cost-benefit analysis to quantify lifecycle, packaging and thermal management.

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